Master of Computer Engineering (MSCE) Curriculum

The Master of Science in Computer Engineering is a 5 trimester program that covers course work, advanced projects and a thesis option (4 Trimesters without a thesis). A total of three (3) courses per trimester are needed. Each course is 3 Units. Hence 45 Units are needed to complete the Master’s program (with thesis, 36 without a thesis). MSCE has a hardware and system focus as opposed to the MSCS which has a software focus. There is some coursework overlap between the MSCE and MSCS programs.

The general pre-requisite for the MSCE is a BSc. in one of the following fields: computer science, computer engineering, electrical engineering, physics, and related fields. If students lack perquisites such as a sound background in computer systems, logic design and programming languages, then an extra trimester is needed to build the appropriate skills.

Curriculum Structure:

1. Logic and Hardware Design (CSE-H-570 series)
2. ASICS and Circuit Design (CSE-H-580 Series)
3. Infrastructure (CSE-I-500 series)
4. Systems (CSE-S-510 series)
5. Communications (CSE-C-520 series)
6. Programming Languages and Algorithms (CSE-P-530 series)
7. Engineering Management (CSE-M-550 series)
8. Business (CSE-B-1000 series)
MSC&E COURSE STRUCTURE

Business
- Engineering Management
- Business Management
- Product Management

Software
- Applications
- Algorithms
- Programming Languages
- Applications

Hardware
- ASICS
- System design
- Logic Design
- Circuits

Foundation
- Data Center Infrastructure
- Computer Systems
- Communications
- Formal Methods

No programming experience
- Programming Language (C/C++/JAVA)
- Computer Architecture & Systems
- Data Structure & Algorithms
SUBJECT: EMBEDDED SYSTEMS (CSE-H-570)
CREDIT HOURS: 3
DURATION: 1 Trimester
TEXT BOOKS: 
PREREQUISITES: 1. Digital Logic Design; Algorithms & programming.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS: ARM Development board, NVIDIA Tegra Dev. Kit. Android OS, Embedded Linux
COURSE OBJECTIVES: Hardware/software systems and co design. Models of computation for embedded systems. System-level design, Modeling, specification, synthesis, and verification. Hardware/software implementation, Design space exploration, Performance analysis and optimization. Multiprocessor system on chip, Platform-based design. Design methodologies and tools. Case studies and design projects.
SEQUENCE OF INSTRUCTION:
1. Hardware/software systems and co design
2. Models of computation for embedded systems
3. Architecture selection
4. Partitioning, scheduling, and communication
5. Simulation, synthesis, and verification
6. Hardware/software implementation
7. Performance analysis and optimization
8. Design methodologies and tools
9. Design examples and tools
GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: DIGITAL SIGNAL PROCESSING (CSE-H-571)
CREDIT HOURS: 3
DURATION: 1 Trimester
RESEARCH PAPERS: IEEE Signal processing magazine, IEEE Transactions on signal processing
PREREQUISITES: Digital Logic Design, C/C++ Programming
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS: Matlab; Texas Instruments Code Composer and DSP development systems.
COURSE OBJECTIVES: This course will provide a broad overview of the current state-of-the-art in DSP design and programming techniques. The presented material will describe DSP offering from leading vendors, applications, and implementations. The course is intended to familiarize the audience with active areas of DSP development, and provide direction for further investigation.
SEQUENCE OF INSTRUCTION:
1. Introduction to digital signal processing: Signal, transducers and sensors, different types of electrical signal, time domain and frequency domain, analogue and digital data, what is DSP, applications of DSP.
2. Conversion of analogue to digital signal: Binary representation of a number, sampling, decibel unit, quantization error, aliasing and anti-aliasing, Niquist frequency criteria, analogue to digital converter.
4. Periodic functions and Fourier synthesis: Periodic functions, time domain and frequency domain, Fourier series (constructing a waveform with sine waves, constructing a waveform with cosine waves, constructing a waveform with both sine and cosine) Gibb’s phenomenon, Fourier theory explained, Fourier transform.
8. DSP systems: Digital signal processor architecture, DSP applications, limitations of DSP.
GRADING SYSTEM:
1. Research Assignments = 25%
2. Projects = 25%
3. Paper Reading & Presentation = 25%
4. Tests = 25%
SUBJECT: LOGIC DESIGN (CSE-H-572)
CREDIT HOURS: 3
DURATION: 1 Trimester


RESEARCH PAPERS: IEEE Circuits & Systems
PREREQUISITES: 1. Digital Logic Design; 2. Algorithm & Computing

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS: Proteus, Verilog HDL, VHDL, Xilinx / Altera boards and tool chains. Synplicity.

COURSE OBJECTIVES: This course presents principles and techniques in logic design: design and analysis of combinational circuits, sequential circuits, state machines and asynchronous circuits. Students will further learn popular HDLs (Verilog and VHDL) for logic design. The knowledge gained from digital circuit design will be applied to principles of architecture, micro architecture, and memory hierarchy in processor design.

SEQUENCE OF INSTRUCTION:

1. Review of Boolean Algebra
2. Combinational-circuit building blocks, such as multiplexers, decoders, encoders, and code converters
3. Karnaugh Maps
4. Sequential-circuit building blocks, such as flip-flops, registers, and counters
5. State machines
6. Synchronous vs. asynchronous circuits
7. HDL tools: Verilog and VHDL
8. Logic simulation and synthesis
9. Processor architecture and micro-architecture
10. Memory sub-systems

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
**SUBJECT:** ADVANCED MICROPROCESSOR ARCHITECTURE (CSE-H-573)  

**CREDIT HOURS:** 3  

**DURATION:** 1 Trimester  


**REFERENCE BOOKS:** Intel Microprocessors, the (8th Edition). Barry B. Brey. 2011.  

**RESEARCH PAPERS:** IEEE Micro, IEEE Computer, IEEE Transactions  

**PREREQUISITES:** 1. Digital Logic Design; 2. Algorithm & Computing  

**MODE OF TEACHING:** 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects  

**TOOLS:** Gem5 Simulator, OPVsim  

**COURSE OBJECTIVES:** The course will examine modern architectures such as Pentium M, Core, and Core 2 Duo and explain concepts such as pipelining, cache hierarchies, memory sub-systems, superscalar processing, instruction decode & execution. Discussion of: Programming fundamentals (arithmetic instructions, memory accesses, control flow instructions, and data types), branch prediction and speculative execution, instruction set architectures, RISC and CISC, bus timing as well as memory and I/O interfaces associated with contemporary microprocessor families. In order to familiarize the designer with the operational aspects of systems based on these processors, the course will involve extensive use of assembly language programming so that system architecture and interface performance can be gauged.  

**SEQUENCE OF INSTRUCTION:**  

1. An overview of Microcomputer Architectures  
2. The Intel Family Architecture  
3. Micro architecture  
4. Instruction fetch, decode and execution  
5. Instruction pipelining and execution order  
6. Memory Management  
7. Bus Structures and Timing Considerations  
8. Memory and Cache  
10. Interrupt Control, I/O Interfaces and DMA  
11. Numeric Processor and Floating point  

**GRADING SYSTEM:**  

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight (%)</th>
</tr>
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<tbody>
<tr>
<td>Research Assignments</td>
<td>20</td>
</tr>
<tr>
<td>Projects</td>
<td>40</td>
</tr>
<tr>
<td>Tests</td>
<td>40</td>
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</table>
SUBJECT: MULTICORE & PARALLEL COMPUTING (CSE-H-574)
CREDIT HOURS: 3
DURATION: 1 Trimester
LECTURES SOURCE: http://www.intel.com/education/highered/Multicore/Multicore.html

Michael J. Quinn. Parallel Programming in C with MPI and Open MP. 2003.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS: Intel Parallel Studio

COURSE OBJECTIVES: The goal of this course is to provide a deep understanding of the fundamental principles and engineering tradeoffs involved in designing modern parallel computers (aka "multiprocessors" and "multicore"), as well as the programming techniques to effectively utilized these machines. Parallel machines are already ubiquitous from desktops to supercomputers, and the expectation is that they will become even more commonplace in the future. Course topics include naming shared data, synchronizing threads, and the latency and bandwidth associated with communication. Case studies on shared-memory, message-passing, data-parallel and dataflow machines will be used to illustrate these techniques and tradeoffs. Programming assignments will be performed on one or more commercial multiprocessors, and there will be a significant course project.

SEQUENCE OF INSTRUCTION:
1. Why Parallel Architecture?
   a. Evolution and Convergence
   b. Fundamental Design Issues
2. Parallel Programming:
   a. Performance
   b. Case Studies
3. Implications for Programming Models
4. Workload-Driven Architecture Evaluation
5. Shared Memory Multiprocessors
6. Directory-Based Cache Coherence
7. Memory Consistency Models
8. Snoop-Based Multiprocessor Design
9. Synchronization
10. Scalable Distributed Memory Multiprocessors
11. Interconnection Network Design
12. Latency Tolerance: Prefetching
13. Latency Tolerance: Multithreading

GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: ADVANCED DIGITAL DESIGN, VERILOG & VHDL (CSE-H-575)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS: Advanced Digital Design with the Verilog HDL, 2/E. Michael D. Ciletti. 2010


RESEARCH PAPERS:

PREREQUISITES: 1. Digital Logic Design

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

TOOLS: Verilog HDL, Xilinx, EDA Tools Cadence, ModelSim

COURSE OBJECTIVES: This course covers topics in the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of logic and system design, synthesis, and optimization for area, speed and power consumption. The course enables students to apply their knowledge for the design of advanced digital hardware systems with corresponding EDA tools. Verilog HDL will be used for simulation and synthesis of the homework assignments and final design project.

SEQUENCE OF INSTRUCTION:

1. Review of Combinational Logic
2. Review of Sequential Circuits
3. Verilog HDL Models and Synthesis
4. Timing Analysis and Optimizations
5. Synthesis and Optimizations
6. Power Analysis and Optimizations
7. The Design of Digital Systems – Examples

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: DIGITAL IC DESIGN (CSE-H-580)
CREDIT HOURS: 3
DURATION: 1 Trimester
Circuits, Interconnects, and Packaging for VLSI, H. Bakoglu, Addison Wesley.
RESEARCH PAPERS: IEEE Circuits & Systems
PREREQUISITES: MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS: Cadence Design System.
COURSE OBJECTIVES: The goals are to understand the principles of digital CMOS integrated circuit design; derive compact and efficient circuit structures to implement digital functions; to introduce the steps used in MOSFET fabrication and begin the study of CMOS circuit and logic design. A laboratory is integrated into the lecture. Students will gain skills in device and small scale integrated circuit simulation, CMOS IC layout, and verification and validation of design specifications. Lecture will focus on behavior of n (p) channel MOS enhancement devices with depletion and zero threshold devices used in some circuits. Scalable (lambda) CMOS design rules are used in the laboratory. Devices models are based on 0.050 (50nm) CMOS n-well technologies.
SEQUENCE OF INSTRUCTION:
1. MOS transistors
2. SPICE simulation
3. VLSI and CMOS processing technologies.
5. Logical effort for delay modeling.
6. Key issues of power dissipation.
7. Dominant role of interconnect (wire) in integrated circuit design.
8. The conversion from the ideal design world to the manufacturing of physical (real) chips.
9. CMOS to design and build digital combinational and sequential logic circuits.
10. Team Design Projects.
GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: ADVANCED DIGITAL IC DESIGN (CSE-H-581)
CREDIT HOURS: 3
DURATION: 1 Trimester
RESEARCH PAPERS: As assigned.
PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
COURSE OBJECTIVES: The development in digital integrated circuit design are continuously moving towards smaller and smaller transistors at the same time as more and more components can be integrated at the same silicon die. The circuit designer is thus facing new problems when new parameters are influencing the design work. Phenomenon like leakage and short channel effects in the transistors are some examples on that. New design methods are therefore required. New technologies will also require new methodologies for test and verification.

Another important area is design of arithmetic building blocks such as adders and multipliers, which are basic operations in many designs. There are a large number of opportunities when implementing digital circuits that give different results on speed, area, and power consumption. Clocking of digital synchronous circuits is an area with increasing problems today. Efficient clocking strategies and alternatives such as asynchronous design are studied.

SEQUENCE OF INSTRUCTION:
1. Transistor Models – Review, Short Channel Devices
2. CMOS Technology and Design Rules, CMOS Inverter
3. Static CMOS Logic Circuits
4. Synchronous Logic, Basic Sequential Circuits, Low Power Design, Performance
5. CAD/Design Flow, Regular Circuit Design Structures
6. ASIC Design Concepts, Arithmetic Blocks and Micro architectures
7. Design for Testability, Memories
8. VLSI in DSP
9. VLSI in Communications
10. The final project involves the design of a microprocessor sub-block at the transistor-level (e.g., 64b adder, 16kb SRAM)

GRADING SYSTEM:
4. Research Assignments = 20%
5. Projects = 60%
6. Tests = 20%
SUBJECT: ANALOG MIXED SIGNAL IC DESIGN (CSE-H-582)

CREDIT HOURS: 3

DURATION: 1 Trimester


Analog Integrated Circuit Design, David Johns, Ken Martin, University of Toronto,

RESEARCH PAPERS: “The Baker ADC – An Overview” Kaijun Li, Vishal Saxena, and Jake Baker


PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

TOOLS: Cadence Design Systems, HSPICE from Synopsys

COURSE OBJECTIVES: The analog/mixed-signal IC design field of study is based on the use of standard fabrication technologies (e.g., CMOS and BiCMOS) to realize analog and mixed-signal functions on monolithic integrated circuits. Pushing standard technologies to the highest possible performance in terms of speed, throughput, power efficiency, density, and signal integrity is emphasized. Students enrolled in this field of study learn practical circuit design techniques as well as device characteristics and the mathematical theory of circuit synthesis and analysis.

Subjects include: op-amps, phase-locked loops (PLL), high-speed RF circuits, high-speed broadband circuits, phase-locked loops (PLL), clock/data recovery (CDR) circuits, analog and optical signal processing, and CMOS digital camera technologies.

SEQUENCE OF INSTRUCTION:

1. Amplifier design: Operation amplifiers, differential amplifiers, operational transconductance amplifiers
2. RF circuits: Low-noise amplifiers, power amplifiers, mixers, oscillators, frequency synthesizers, RF transceivers.
3. Broadband circuits: Phase-locked loops (PLL), clock/data recovery (CDR) circuits, serializers/deserializers, adaptive equalizers, broadband transceiver architectures.
4. CMOS imaging: CMOS digital camera technologies, analog to digital converters, digital to analog converters low-noise techniques, focal-plane memory and processing.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
VLSI PHYSICAL DESIGN-PLACEMENT & ROUTE (CSE-H-583)

SUBJECT: VLSI PHYSICAL DESIGN-PLACEMENT & ROUTE (CSE-H-583)

CREDIT HOURS: 3

DURATION: 1 Trimester


RESEARCH PAPERS: http://www.mentor.com/products/ic_nanometer_design/

PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects


COURSE OBJECTIVES: This course is the third in the VLDI Design series and it introduces ASIC place and route. The course introduces the students to state-of-the-art physical design automation tools and techniques. Topics include design flow, library review, tool graphical interface, floor planning, power planning, timing driven placement, static time analysis (STA), CT-Gen, special routing, final routing, and engineering change order (ECO), and run batch mode jobs. Hands-on exercises and projects are required.

SEQUENCE OF INSTRUCTION:

1. Intro & Physical Design
2. Timing Analysis & Timing Optimization
3. Floor planning, Partitioning & Placement
4. Routing & Compaction
5. Introduction to Combinational Logic Optimization
6. Technology Mapping
7. Review of key algorithmic concepts in CAD
8. Sequential Circuit Design
9. Verification
10. Manufacturing Test
11. RTL and Behavioral Synthesis
12. Programmable Platforms
13. Architectural Platforms
14. Mapping Applications into Architectures

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN (CSE-H-584)
CREDIT HOURS: 3
DURATION: 1 Trimester
RESEARCH PAPERS: As assigned.
PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
TOOLS:

COURSE OBJECTIVES: This is the second in a two course sequence focused on the design and analysis of VLSI integrated circuits from a system design perspective. This is a project-oriented course in the field of Very Large Scale Integration (VLSI) circuit design. Design and analysis of Application-Specific Integrated Circuits (ASICs) will be covered from the circuit and system design perspectives. A quarter-long, high-complexity project will be assigned to students working in teams. Team-work, task assignment and team communication will be mediated in an industry setting, stimulating a realistic design environment. Design tasks will cover the physical IC design flow range, from RTL description to manufacturing. Successful designs will be sent to MOSIS for fabrication.

SEQUENCE OF INSTRUCTION:
1. CMOS gate review, Delay in CMOS overview
2. Cell types in 260
3. Latches and FFs
4. The clock cycle and paths
5. Working with latches
6. Multiple clock Domains
7. Fifos, Fixing Long Paths and Races
8. Working with timing
9. A real library, Delay models
10. Timing closure, Clock distribution networks
11. Product debug requirements
12. I/O pads and packaging
13. Power and Ground pins, Power estimation
14. Floor plan and impacts
15. Manufacturing and test D algorithm
16. Scan based testing & D algorithm

GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: HIGH SPEED DIGITAL SYSTEM DESIGN (CSE-H-585)
CREDIT HOURS: 3
DURATION: 1 Trimester

RESEARCH PAPERS:

PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

SOFTWARE TOOLS:

COURSE OBJECTIVES: This module aims to equip the student with a range of techniques applicable to the design and test of very high speed and fault-tolerant digital circuits. The course line includes High-speed digital system design, Transmission lines, Clock distribution & buffering, Fault-tolerance & redundancy.

SEQUENCE OF INSTRUCTION:

1. High-speed design in the time and frequency domains; reflection, ringing and crosstalk, transmission lines.
2. Transmission lines and termination strategies: Series, Thevenin’s theorem, diode and AC terminations; Crosstalk, reflections, ground bounce.
3. Properties and behavior of strip line and micro strip traces.
4. Technology review: LVDS, ECL/PECL, GTL, SSTL, HSTL, and high-speed CMOS drivers and receivers; mixed voltage systems; bus-hold and bus-loading considerations; hot insertion.
5. Synchronous Design: Clock oscillators and buffering, Clock Distribution, Metastability.
6. System Design and Manufacture: PCB materials; Layer build and specification; Power supply considerations; Decoupling techniques.
7. EMC/ESD: Radiated vs. conducted; Filtering; Effects of apertures, gasketing; Conducted emissions, coaxial cables, twisted pair; Shielding.
8. Thermal Aspects: Sources of heat; Thermal resistance; Basic airflow models; Impact on reliability; Altitude Effects.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: SIGNAL INTEGRITY IN ADVANCE IC PACKAGING & PCB DESIGNING (CSE-H-586)

CREDIT HOURS: 3

DURATION: 1 Trimester


RESEARCH PAPERS: 

PREREQUISITES: Digital IC Design, MOS ICs, logic and analog simulation CAD tools, basic layout geometry of MOS ICs.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

TOOLS: 

COURSE OBJECTIVES: This course is designed to build on the knowledge and skills accumulated in the previous courses Digital Circuit Design and VLSI. The course is fast-paced and covers complex topics in depth, expanding on details and complexities of the circuit types, as well as new and advanced topics such as standard cell libraries, data path design and layout, analog circuits, etc. There is increased attention to more in-depth exploration of the tool environments: Virtuoso library / technology setup, and verification tools such as Diva, Dracula and Caliber. Introductory use of schematic Composer, Virtuoso XL and some Cadence Skill programming is also covered.

SEQUENCE OF INSTRUCTION: 

1. Getting Started with AutoCAD
2. Design Center and Tool Palettes
3. Simple Schematics Designs using AutoCAD
4. Intermediate Schematic Designs using AutoCAD
5. Advanced Schematic Designs using AutoCAD
6. Intro to PCB design
7. Intro to a commercial PCB design software
8. Compromise between PCB board size and component sizes in design layouts
9. Design of 2-layer (PCB layer) PCB boards.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
IMAGE PROCESSING AND APPLICATIONS (CSE-H-587)

CREDIT HOURS: 3

DURATION: 1 Trimester


RESEARCH PAPERS:

PREREQUISITES: Experience with C/C++ or Matlab. A course on Digital Signal Processing.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

TOOLS: Matlab,

COURSE OBJECTIVES: This is an advanced senior and graduate level elective course on Digital Image Processing, which provides a comprehensive theory of various image processing tasks and the practical experience to simulate them. Upon the completion of this course, the students will have gained a hands-on experience about the below topics through extensive simulation assignments.

SEQUENCE OF INSTRUCTION:

1. Digital Image Fundamentals; Human visual system; Sampling and Fourier analysis
2. Intensity Transformations and Spatial Filtering, Histogram Processing, Spatial Filtering
3. Filtering in the Frequency Domain, Preliminary Concepts, Extension to functions of two variables, Image Smoothing, Image Sharpening
4. Image Restoration and Reconstruction, Noise Models, Noise Reduction, Inverse Filtering, MMSE (Wiener) Filtering
5. Color Image Processing, Color Models, Color Transforms, Image Segmentation Based on color
6. Image Compression, Fundamentals, Basic Compression Methods
7. Morphological Image Processing, Erosion, dilation, opening, closing
8. Basic Morphological Algorithms: hole filling, connected components, thinning, skeletons
9. Image Segmentation, Point, line, edge detection, Thresholding, Region-based segmentation

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
CIRCUIT THEORY - I (CSE-H-588)

CREDIT HOURS: 3

DURATION: 1 Trimester


REFERENCE BOOKS: Engineering Circuit Analysis by Hayt, Kimmerly and Durbin, McGrawHill

RESEARCH PAPERS:

PREREQUISITES: Basic Physics of electronics component would be helpful.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

TOOLS: PSpice, Proteus

COURSE OBJECTIVES: The course aims is to explain the working principles of resistors, capacitors and inductors in terms of voltage and current. Ohm’s law, KCL and KVL are explained in detail. In summary, the course prepares a student to solve basic electric circuits consisting of the above mentioned passive/active circuit elements. Each theory topic is supplemented with appropriate lab experiment. This course prepares the students for more advanced courses in electronic engineering to follow in subsequent semesters.

SEQUENCE OF INSTRUCTION:

1. Basic Circuit Elements
2. Ohm’s law
3. KCL & KVL
4. Node & Loop Analysis
5. Series & Parallel Circuits
6. Linearity & Superposition Principles
7. Network Laws like Thevenin’s Theorem & Norton’s Theorem
8. Maximum Power Transfer Theorem
9. Transformers and Amplifiers
10. Operational Amplifiers
11. Summing and Differencing Amplifiers
12. Transresistance, Transconductance and Current Amplifiers
13. Inductive & Capacitive Circuits

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: CIRCUIT THEORY - II (CSE-H-589)
CREDIT HOURS: 3
DURATION: 1 Trimester
REFERENCE BOOKS: Engineering Circuit Analysis by Hayt, Kimmerly and Durbin, McGrawHill
RESEARCH PAPERS:
PREREQUISITES: Circuit Theory – I & Basic Physics of electronics component would be helpful.
MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects
SOFTWARE TOOLS: PSpice, Proteus

COURSE OBJECTIVES: The course focuses on the analysis and circuit’s response of First and Second Order Circuits by formulation of the differential equation of the circuit and its solutions for DC and AC Forcing Functions. The concept of phasors and Laplace transformation are introduced as a tool to solve the circuit equations in Laplace and Phasor Domains. The course also covers the frequency response of a circuit through sinusoidal analysis.

SEQUENCE OF INSTRUCTION:
1. Natural response of 1st order circuits
2. 1st order circuits with dependent sources
3. Response of 1st order circuits to constant forcing function
4. Response of 1st order circuits to non-constant forcing function
5. Complete response of 2nd order circuits
6. Laplace transform and inverse Laplace transform
7. Solving Circuit differential equations using Laplace transform
8. Laplace transform of special signals
9. Direct transformation of circuits in to s-domain
10. AC steady state power
11. Concepts of average power, complex power and power factor
12. Frequency response of 1st order circuits
13. Asymptotic magnitude and phase Bode plots

GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
SUBJECT: SIGNALS AND SYSTEMS (CSE-H-590)

CREDIT HOURS: 3

DURATION: 1 Trimester


REFERENCE BOOKS: Signals, Systems & Transforms, By Charles Philips, John M. Parr Prentice Hall.

RESEARCH PAPERS:

PREREQUISITES: Nil

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations; 3. Labs & Projects

SOFTWARE TOOLS: Matlab

COURSE OBJECTIVES: This course is an introduction to basic concepts and principles of signals and systems. Both analog and digital signal processing techniques will be covered. Topics include analog signals and systems, digital signals and systems, LTI systems, Fourier transform, Z-transform, FFT, system stability, digital filter design, Network. Matlab software will be used to implement some of the DSP algorithms.

SEQUENCE OF INSTRUCTION:

1. Fundamentals of Signals and Linear time Invariant systems.
2. Time domain signal analysis and different properties of LTI systems.
3. Frequency domain (Fourier Domain) signal analysis and different properties of LTI systems.
4. Periodicity of the signals and difference between Fourier series and Fourier Transform.
5. continuous time signal processing & its
6. Discrete time signal processing.
7. Laplace Transform and its properties.
8. Fourier and Laplace Transforms in the areas of advance courses of signal processing.
9. Understand the basic concepts of Analog Filter Design.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 60%
3. Tests = 20%
COURSE NAME: Enterprise Data Center Architecture (CSE-I-501)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS: Enterprise Data Center Design and Methodology. Rob Snevely.
VMware ESX Essentials in the Virtual Data Center by David Marshall, Stephen S. Beaver and Jason McCarty

REFERENCE BOOKS: Data Center Fundamentals. Mauricio Arregoces, Maurizio Portolani


MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: This course instructs students in specification, design, implementation and management of enterprise data centers. Enterprises data centers employ components such as power management, servers, virtualization, storage and networking equipment. Candidates will learn to configure and manage industry standard equipment such as Red Hat Linux, MS Windows, Oracle databases, Cisco routers and switches etc.

SEQUENCE OF INSTRUCTION:

1. Methodology for designing data centers of any size and capability
2. Design techniques for accurate planning based on data center capacities
3. Power management
4. Managing Linux, Windows servers
5. Managing virtual systems
6. Configuration and management of databases: Oracle, MS SQL, MySQL
7. Network connectivity, configuring and managing switches and routers.

GRADING SYSTEM:

10. Research Assignments = 20%
11. Projects = 30%
12. Paper Reading & Presentation = 10%
13. Tests = 40%
COURSE NAME: Cloud Data Center Architecture (CSE-I-502)
CREDIT HOURS: 3
DURATION: 1 Trimester


MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Cloud computing has evolved as a very important computing model, which enables information, software, and shared resources to be provisioned over the network as services in an on-demand manner. Data centers that consolidate data processing and storage capabilities have emerged as the major infrastructure for supporting cloud computing. Virtualization has and will continue to play a key role in modern data centers. This graduate-level course covers advanced topics on cloud computing and data centers, with emphasis on data center networking and virtualization. Homework assignments and a project assignment will be given to help student develop a better understanding of data center networking technologies, and practice Virtual Machine (VM) creation, configuration and programming. After taking this course, the students are expected to know the state-of-the-art in architectures, software, algorithms and protocols related to cloud computing and data centers, and more importantly, to understand how scientific research is done. Practical aspects will cover offerings form Amazon, Microsoft, Google and Software as a service solution such as Salesforce.com.

SEQUENCE OF INSTRUCTION:
1. Review for networking basics and TCP/IP
2. Introduction to cloud computing
3. Introduction to data centers: servers, data storage, networking and virtualization
4. Data center networking: Ethernet, network topologies, routing, addressing,
5. transport layer protocols, etc
6. Introduction to server virtualization software: VMware VSphere
7. Virtual machine management: configuration, placement and resource allocation.
8. Power efficiency & fault tolerance in virtual data centers
9. Amazon EC2, Microsoft Azure, Google AppEngine, Facebook Casandra, Hadoop

GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 40%
3. Paper Reading & Presentation = 20%
4. Tests = 20%
COURSE NAME: Storage Systems (CSE-I-503)

CREDIT HOURS: 3

DURATION: 1 Trimester


REFERENCE BOOKS: Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel and IP SANs, 2nd Edition, Tom Clark, Addison Wesley Professional

PREREQUISITES: UNIX/Linux and C/C++ programming

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: One of the biggest challenges facing IT departments in businesses around the world is setting up or finding the best storage system for their data. This course looks at the local and network protocols to develop storage systems, transports such as iSCSI, FC, InfiniBand and file system protocols such as NFS, CIFS and XFS. It is important for students to know how to manage storage systems across heterogeneous settings. The course will cover the design and implementation of storage systems and the architecture and characteristics of the components on which storage systems are built. Topics will range from the device level up to distributed systems concepts. Projects will be around offerings from EMC, NetApp, Microsoft and other storage management vendors.

SEQUENCE OF INSTRUCTION:

1. Disk drive hardware and firmware
2. File system and database structures
3. Mirroring and RAID
4. Disk array controllers
5. Local storage interconnects
6. Storage area networks
7. Capacity planning and configuration
8. Distributed file systems and network-attached storage
9. Backup/restore and disaster recovery
10. Security for storage.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Computer System Architecture (CSE-S-510)

CREDIT HOURS: 3

DURATION: 1 Trimester

By John L. Hennessy and David A. Patterson


PREREQUISITES: Understanding of CPU, memory and I/O subsystems

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: This course provides a systematic study of core concepts of computer architecture design. These concepts have been developed in the last 50+ years, guided by extraordinary technology advancements, and the constant designer effort to get maximum performance out of desktop computers while minimizing the cost. The main focus is on key principles for high-performance low-cost desktop design. It covers in detail instruction set architectures, pipeline architecture, cache and virtual memories, methods for exploiting instruction level parallelism, multiprocessors and I/O devices.

SEQUENCE OF INSTRUCTION:

1. Performance and ISAs
2. ISAs and Role of Compilers
3. MIPS Overview, Pipeline, Hazards, Multi cycles
4. Instruction Level Parallelism (ILP)
5. Dynamic Scheduling: Scoreboard
6. Dynamic Scheduling: Tomasulo
7. Hardware Speculation
8. Study of the Limitations of ILP
9. Cache, Virtual Memory
10. Multiprocessors and Thread-Level Parallelism; Symmetric Shared Memory
11. Distributed Shared Memory
12. Memory Technology; Virtual Memory and Virtual Machine
13. Design of Memory Hierarchy

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Operating Systems (CSE-S-511)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: Understanding of CPU, memory and I/O subsystems hardware and software.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: The course will cover the major components of modern operating systems. This discussion will cover the tradeoffs that can be made between performance and functionality during the design and implementation of an operating system. Particular emphasis will be given to three major OS subsystems: process management (processes, threads, CPU scheduling, synchronization, and deadlock), memory management (segmentation, paging, swapping), and file systems. Further topics cover operating system support for clustered computing, distributed system multiprocessor platforms and security.

SEQUENCE OF INSTRUCTION:

1. CPU & computer system architecture overview
2. Processes, Threads
3. CPU Scheduling
4. Process Synchronization
5. Main Memory & Virtual Memory
6. File System Interface & Implementation
7. Mass Storage Structure
8. I/O Systems
9. Distributed File System & Distributed Coordination

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Computer and Information Security (CSE-S-512)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: Understanding of CPU, memory and I/O subsystems, Algorithms

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: The objectives of this course are to provide an overview of the need for, and the technology, algorithms, and standards used in providing computer and communications security. The class is concerned with the fundamentals of computer security. Topics in this class can be divided into three main parts: cryptography (with a focus on single-key and public key), computer system security (database and operating systems issues including authentication, access control, malicious software); as well as network security (including intrusion prevention/firewalls, intrusion detection, Denial of Service attacks, etc.), and writing secure programs.

SEQUENCE OF INSTRUCTION:
1. Introduction to Course & Computer Security Overview
2. Classical Cryptography
3. Modern Symmetric Cryptography
4. Public Key Cryptography
5. User Authentication
6. Access Control
7. Database Security
8. Malicious Software
9. Denial of Service; Intrusion Prevention/Firewalls
10. Secure Software Development

GRADING SYSTEM:
1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Databases (CSE-S-513)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: Understanding of CPU, memory and I/O subsystems, Algorithms

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: This course covers fundamentals of database architecture, database management systems, and database design and application development. Practical aspects will cover solutions from vendors such as Oracle and SAP.

SEQUENCE OF INSTRUCTION:

1. Database Environment & Development Process
2. Modeling Data in the Organization
3. Enhanced E-R Model and Business Rules
4. Logical Database Design and the Relational Model
5. Physical Database Design and Performance
6. The Software Engineering Process and Relational Databases
7. Advanced SQL
8. Client/Server, Internet Database Environment
9. Data Warehousing, Creating and Populating Tables
10. SQL Query Development and Derived Structures
11. SQL Set Operations, SQL Correlated Sub queries
12. SQL Indexes and Constraints on Tables
13. Data and Database Administration
14. Distributed Databases
15. Object-Oriented Data Modeling
16. Object-Oriented Database Development

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Modeling, Simulation and System Performance (CSE-S-515)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS: Queuing Modeling Fundamentals: With Applications in Communication Networks, Professor Chee-Hock Ng, Professor Soong Boon-Hee.


PREREQUISITES: Programming Skills in C/C++, Java

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Fundamentals and techniques for designing and using simulation, modeling and optimization algorithms with applications in computer system performance modeling, business infrastructure modeling, modeling networks and client server applications.

SEQUENCE OF INSTRUCTION:

1. Handling Stepped and Event-based Time in Simulations
2. Discrete versus Continuous Modeling
3. Numerical Techniques
4. Sources and Propagation of Error
5. Graph or Network Transitions Based Simulations
6. Actor Based Simulations, Mesh Based Simulations
7. Hybrid Simulations
8. Partitioning the Data
9. Partitioning the Algorithms
10. Handling Inter-partition Dependencies
11. Introduction to Queues and Random Noise
12. Random Variants Generation
13. Sensitivity Analysis
14. Display Forms: Tables, Graphs, and Multidimensional Visualization
15. Validation of Model Results

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Data Communications-I (CSE-C-520)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS: Computer Networks, Andrew S. Tanenbaum, Prentice Hall


REFERENCE BOOKS: Forouzan, Data Communications and Networking, McGraw Hill, 4th Ed.

PREREQUISITES: Operating systems; background in C and UNIX

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: This course examines the underlying technology that makes data communication possible. The course will cover various transmission media, digital and analog signals, modulation, multiplexing, circuit switching, error control and flow control. The course will also cover many real-world examples of data communication, including modems, DSL, Ethernet, wireless LANs, and cell phones. The course focuses on the design of individual networks, but it does finish with a brief overview of internetworking and the TCP/IP internet protocol.

SEQUENCE OF INSTRUCTION:

1. Introduction
2. Fundamentals of information transmission and coding
3. Link Layer technologies. Wired & wireless media
4. OSI 7 Layer model
5. End-to-end communication: packet switching and circuit switching
6. Socket programming and network communication
7. Internetworking with TCP/IP: structure, functionality
8. Congestion control
9. Routing protocols: IPv4, IPv6, RIP, OSPF, IS-IS, EIGRP
10. Application protocols
11. Multimedia protocols: RTSP, VoIP.
12. Transparent network services: DNS, HTTP, web server design, caching and CDNs

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Data Communications-II (CSE-S-521)
CREDIT HOURS: 3
DURATION: 1 Trimester

Mobile WiMAX: A Systems Approach to Understanding IEEE 802.16m Radio Access Technology. Sassan Ahmadi

REFERENCE BOOKS: Wireless and mobile network architectures by Lin, Jason Yi-Bing; Chlamtac, Imrich

PREREQUISITES: Data Communication-I (CSE-S-520)

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations


SEQUENCE OF INSTRUCTION:

1. To learn wireless local area networks based on IEEE 802.11 standard
2. Apply Wireless LAN layer 2 functions and operations for media access and control.
3. Understand power conservation operations for multicast and broadcast modes.
4. Determine mobile networks QoS (Quality of service) requirements.
5. Apply IEEE 802.11e (QoS for WLAN), and IEEE 802.11k (transmit power control).
6. To learn ZigBee IEEE 802.15.4 standard.
7. Understand WiMax IEEE 802.16 networks
8. To learn the cellular technology concepts of GSM, GPRS, UMTS, WCDMA, HSDPU, HSDPA.
9. Understand base station transceiver configuration types.
10. To learn the concept of SS7 (Signaling System 7) protocol for PSTN.
11. Understand the concept of satellite communication networks; ground segment, space segment, control segment, access methods, protocols, interconnection of coverage areas.
12. To conduct independent project and to equip for scholarly research and industrial product development in wireless mobile networks.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Formal Specification Techniques (CSE-P-530)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: Understanding of programming languages

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Advancements in technology have led to more formalized specifications in multiple areas. Therefore, it is crucial students obtain a working knowledge of formal specification techniques so they are able to choose the best model possible. This course focuses on the formal specifications of systems and software and provides instruction on how to use tools and methodologies to determine the best formal specification for the situation.

SEQUENCE OF INSTRUCTION:

1. (Introduction): who, what, why
2. (PC): Propositional Calculus
3. (OBDDs): Ordered Binary Decision Diagrams
4. (LPC): Predicate calculus -- the machine code of reality
5. (CTL): Dynamic Logic
6. (SMV): Tool
7. (Hoare): Verifying programs

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Advanced Data Structures and Algorithms (CSE-P-531)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: Data structures and algorithms, programming experience.

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Study efficient algorithms for a number of fundamental problems, learn techniques for designing algorithms using appropriate data structures, prove correctness and analyze running times of algorithms.

SEQUENCE OF INSTRUCTION:

1. Amortized complexity
2. External sorting & tournament trees
3. Buffering
4. Run generation & optimal merge patterns (Huffman trees)
5. Priority queues and merging
6. Leftist trees, Binomial heaps and Fibonacci heaps
7. Pairing heaps
8. Double ended priority queues
9. Static and dynamic weighted binary search trees
10. AVL-trees, Red-black trees, Splay trees, B-, B+- and B*-trees
11. Tries and digital search trees, Tries and packet forwarding, Suffix trees
12. Bloom filters
13. Segment trees, Interval trees, Priority search trees
14. k-d trees, Quad and Octal trees, BSP trees, R-trees

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Compilers and Languages (CSE-P-532)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS: Compilers: Principles, Techniques, and Tools by Aho, Alfred V.; Lam, Monica S.; Sethi, Ravi; Ullman, Jeffrey D.

REFERENCE BOOKS:

PREREQUISITES: An advanced course on data structures and an introductory course on assembly language programming

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Introduction to formal language concepts: regular expressions and context-free grammars. Compiler organization and construction. Lexical analysis and implementation of scanners. Top-down and bottom-up parsing and implementation of top-down parsers. An overview of symbol table arrangement, run-time memory allocation, intermediate forms, optimization, and code generation

SEQUENCE OF INSTRUCTION:

1. Build a compiler for a nontrivial programming language.
2. Explain the phases of compilation.
3. Specify regular expressions for matching tokens in a language.
4. Show the equivalence between regular expressions, NFAs, and DFAs.
5. Specify and disambiguate context-free grammars.
6. Specify a type system for a language including type equivalence, and use it to correctly type check expressions in a language.
7. Apply fundamentals of storage allocation strategies toward run-time management of data.
8. Generate correct assembly code for simple expressions and statements in a programming language.

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Technical Writing and Presentation (CSE-M-550)

CREDIT HOURS: 3

DURATION: 1 Trimester


PREREQUISITES: B. Sc. in Engineering or Science

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: Issues of technical writing and effective presentation of technology and business topics. Preparation of documentation, papers, books, and computer programs. Students will build expertise in how to write technical papers for industry and academic publications, project plans, business plans, and executive presentations

SEQUENCE OF INSTRUCTION:

1. Effective use of library & online resources, copyrights, trademarks, etc.
2. Technical papers, academic publication
3. Business communication, project plans, business plans, executive presentations
4. Writing style, editing, and formatting; including graphs, figures, and tables
5. Developing effective time lines and reasonable budgets
6. Literary review/critique of professional article/text
7. Research ethics and separation of good/bad science
8. Scientific research methods, analysis, and reporting
9. Development of ideas into a research program
10. Design and analysis of controlled experiments/simulations
11. Interpretation of experimental results
12. Literature search culminating in a research paper
13. Formal presentation of research investigation/project
14. Oral defense of their methods and findings

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME: Program Management (CSE-M-551)

CREDIT HOURS: 3

DURATION: 1 Trimester

TEXT BOOKS:
- The Handbook of Program Management: How to Facilitate Project Success with Optimal Program Management. James T Brown (Author)
- Information Technology Project Management. Kathy Schwalbe

PREREQUISITES: B. Sc. in Engineering or Science

MODE OF TEACHING: 1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES: This course is specifically designed to provide the knowledge and techniques required to properly manage projects of all types and sizes. Course material covers the approaches and practices in project management over the lifespan of the project cycle.

SEQUENCE OF INSTRUCTION:

1. Class Logistics and Introduction; Review of Project and Project Management Definitions and Terminology, Project Planning and Control Techniques; Case Study.
2. Project Organization; Teamwork Exercise, Team Management; Major Management Theories, Leadership, Understand Individuals; Power & Influence;
3. Risk Management; Decision making; Team Project Presentation, Other topics in Project Management
4. Project plan development
5. A project proposal presentation

GRADING SYSTEM:

1. Research Assignments = 20%
2. Projects = 30%
3. Paper Reading & Presentation = 10%
4. Tests = 40%
COURSE NAME:  Engineering Management (CSE-M-552)
CREDIT HOURS:  3
DURATION:  1 Trimester
REFERENCE BOOKS:  Effective Project Management: Traditional, Agile, Extreme. Robert K. Wysocki
PREREQUISITES:  B. Sc. in Engineering or Science
MODE OF TEACHING:  1. Lectures; 2. Research Papers Reviews & Presentations

COURSE OBJECTIVES:  To gain an understanding and appreciation of the fundamental principles and methodologies relevant to planning, design, operation, and control of a world-Class software development effort. Students will get an understanding of the role and importance of productivity how to increase productivity and quality for competing in today's global marketplace. To reinforce analytical skills already learned, and build on these skills to further increase your "portfolio" of useful analytical tools. To gain some ability to recognize situations in a production system environment that suggests the use of certain quantitative methods to assist in decision making.

SEQUENCE OF INSTRUCTION:
1. Introduction to Planning, Nature and Purpose of planning
2. Types of Plans
3. Latest software on Planning
4. Case studies in planning
5. Introduction to Planning, Scheduling and Control of Projects
6. Probabilistic and Deterministic Approaches,
7. Gantt, PERT and CPM charts
8. Planning a software project,
9. Determination of Resources Requirements of a Project,
10. Work breakdown structure (WBS)
11. Resource Leveling
12. Project Scheduling Under Limited Resources,
13. Gathering software requirements and creating use cases
14. Improving programming with refactoring, unit testing, and version control
15. Managing an outsourced project
16. Testing software

GRADING SYSTEM:
1. Research Assignments  =  20%
2. Projects  =  30%
3. Paper Reading & Presentation  =  10%
4. Tests  =  40%
SUBJECT: PROJECT & THESIS (CSE-B-1000)

CREDIT HOURS: 3

DURATION: 1-2 Trimesters

Graduate Project Procedure: In order to graduate, each graduate student must complete graduate Project & Thesis. A graduate project is a 3-credit course that must be taken by a student with a graduate faculty. The following policies and procedures must be followed by a graduate student and must be insured by the graduate faculty.

A graduate project serves the purpose of providing applied skills to the student. That means, graduate project should be focused on implementation and learning skills for the student. The graduate project can also be based on survey of current topics in a given field of study and write a paper for publication. Graduate faculty plays a role of training the student to write a proposal, analyze a problem, collect requirements for a problem, design, implement, test, and demonstrate a chosen problem.

Types of Graduate Projects: Many types of topics can be chosen to conduct a graduate project. The graduate faculty is responsible to offer such project based on his/her research interests and need to enhance the student’s applied skill in a chosen topic in computer science. A project should be based on some programming implementation and a computer application that provides the student with applied skills. Some projects such as survey papers, analytical studies that may result in paper publications are also allowed. Topics and projects already done by the student in other courses must be avoided. The graduate faculty is the best judge for making such decisions before accepting for a project study.

Allow to include conceptual analysis of literature or software which requires synthesis, integration, and critical analysis of sources (for example, survey papers). The project report in such cases should be in a publishable paper format.

Project Initiation: A graduate student must initiate a graduate project proposal in collaboration with a graduate faculty. A graduate student can only start a project after completion of 21 credits in the graduate program or the student is graduating during a semester in which he/she is expected to complete all courses towards the degree. The graduate student must write this proposal in consent with the graduate faculty and approval. The student must submit this proposal to the graduate faculty and the faculty in turn will submit it to the graduate program director for approval. The graduate committee must review each proposal and notify the graduate faculty about its decision. The graduate program director must coordinate the entire process. The proposal must be given to the director at least one week before the committee’s meeting. The graduate program director must discuss the proposal with the committee and process it for approval.

Project Proposal Approval Policy:

A project proposal written for course CSE-B-1000 must be approved based on the following conditions.

1. Style, format, readability, and understandability of the proposal (if the graduate committee cannot understand the proposal, it is unlikely that the student will understand it and do a good job in implementation!
2. Technical content and merit of the proposal.
3. Topics to be studied cannot be trivial and already studied in other courses taken by the student.
4. The student finished 21 credits in graduate courses or graduating in the semester in which the graduate project will be registered.

The committee will evaluate proposals based on the above three measures and provide a feedback to the corresponding faculty and student. This process is merely to insure quality of projects and teach our students to write good proposals, clearly define projects, understand project motivation, and consider feasible implementations to complete their projects.
Procedure for Graduate Project Presentation:

Each student must prepare and deliver the following document to members of the Graduate Faculty who are going to attend the presentation and to the project advisor, at least one week before the presentation is scheduled. The document must include the following (for an implementation type project):

1. Problem specification/definition (1-3 pages)
2. System/software architecture, if applicable (1-2 pages)
3. Requirement Specification [software and hardware, if applicable] (6-20 pages)
4. Design specification (6-20 pages)
5. Test cases and test results [if any software has been developed] (5-10 pages)
6. Source code, if any software has been developed (as many pages as needed)

The presentation must be scheduled such that at least two graduate members can attend the presentation. At least two members of the Graduate Faculty will attend each presentation and will evaluate the project as acceptable or not acceptable. The project advisor will give letter grade ("A" or "B") to acceptable projects and "I" to unacceptable projects.

Project Submission:

The graduate project must be submitted in accordance with the following procedure.

1. Once the project is complete, the graduate faculty advising the student must inform the graduate student to complete the rest of this process.
2. Graduate student must write a graduate report and provide one copy for each of the faculty who will attend his/her presentation. At least one faculty from the graduate committee and one other faculty from computer science department must attend the presentation.
3. Graduate student must arrange seminar for an hour to present the topic in presence of his/her graduate faculty and two other faculties as mentioned above.
4. Graduate student must organize the seminar to present the topic and also present a demo to illustrate project work.

Project Evaluation:

The graduate project presented by the graduate student is subject to the following evaluation process:

1. The graduate project must be evaluated based on the graduate student's original proposal and any justifiable changes made since the original proposal.
2. The project must be evaluated based on its technical merit and student's efforts in the project.
3. The graduate faculty project adviser and two other faculties must agree on approving/disapproving the proposal at the end of the presentation.
4. In case of disapproval, the graduate student should be advised to improve the project content and resubmit the project.
5. The graduate student must earn a grade of B or above to complete his project course

NOTE: The graduate advisor is the sole authority for assessment of the grade for the project.